IN THE CLAIMS

1.-10. (Cancelled)

11. (Currently Amended) A semiconductor die comprising:

a substrate having a first planar surface having circuitry thereon surrounded by an unused reduced width buffer area;

a second planar surface opposite the first planar surface;

one or more planar perimeter side surfaces, each planar perimeter side surface extending from the first planar surface to the second planar surface;

and

each planar perimeter side surface of the semiconductor die being a ground or polished surface without substantially any irregularities that produce weak points in the substrate.

12. (Original) The semiconductor die as recited in claim 11, wherein each planar perimeter side surface is transverse to the first planar surface and the second planar surface.

13. (Original) The semiconductor die as recited in claim 11, wherein the semiconductor die has a substantially rectangular shape.

14. (Original) The semiconductor die as recited in claim 11, wherein each planar perimeter surface is a ground surface.

15. (Currently Amended) A semiconductor die comprising:

a substrate having a first planar surface having circuitry thereon surrounded by an unused reduced width buffer area;

a second planar surface opposite the first planar surface;

one or more planar perimeter side surfaces, at least one of the planar perimeter side surfaces extending from the first planar surface to the second planar surface, the entire at least

one perimeter side surface having a ground or polished surface without substantially any irregularities that produce weak points in the substrate.

16. (Original) The semiconductor die as recited in claim 15, wherein each planar perimeter side surface is transverse to the first planar surface and the second planar surface.

17. (Original) The semiconductor die as recited in claim 15, wherein each planar perimeter side surface comprises a polished surface.

18. (Currently Amended) A semiconductor die comprising:

a substrate having a first planar surface having circuitry thereon surrounded by an unused reduced width buffer area;

a second planar surface opposite the first planar surface;

one or more perimeter side surfaces extending between the first planar surface and the second planar surface; and

at least one perimeter side surface having at least two offset planar surfaces, where the at least two offset planar surfaces are substantially parallel to each other and are ground or polished surfaces without substantially any irregularities that produce weak points in the substrate.

19. (Original) The semiconductor die as recited in claim 18, wherein the semiconductor die comprises a rectangular die.

20. (Original) The semiconductor die as recited in claim 18, wherein each perimeter side surface has offset planar surfaces.

21. (Original) The semiconductor die as recited in claim 18, wherein the at least two offset planar surfaces are transverse to the first planar surface and the second planar surface.

22. (Currently Amended) A semiconductor die comprising:

a substrate having a first planar surface having circuitry thereon surrounded by an unused reduced width buffer area;

a second planar surface opposite the first planar surface;

one or more perimeter sides;

and

at least one of the perimeter sides having at least two offset planar surfaces that are substantially parallel to each other and that are ground or polished surfaces without substantially any irregularities that produce weak points in the substrate ~~to remove irregularities from each of the two offset planar surfaces~~.

23. (Previously Presented) The semiconductor die as recited in claim 22, wherein each of the two offset planar surfaces is transverse to the first planar surface and the second planar surface.

24. (Previously Presented) The semiconductor die as recited in claim 22, wherein at least one of the two offset planar surfaces extends from at least one of the first planar surface and the second planar surface.

25. (Currently Amended) A semiconductor die comprising:

a substrate having a first planar surface having circuitry thereon surrounded by an unused reduced width buffer area;

a second planar surface opposite the first planar surface;

one or more perimeter sides extending between the first planar surface and the second planar surface;

each perimeter side having offset perimeter planar surfaces, where the offset perimeter planar surfaces are substantially parallel to each other with one of the offset perimeter planar surfaces extending from the first planar surface and another of the offset perimeter planar surfaces extending from the second planar surface, and each of the offset perimeter planar

surfaces is a ground or polished surface without substantially any irregularities that produce weak points in the substrate.

26.-34. (Cancelled)

35. (Currently Amended) A semiconductor die comprising:

a substrate having a first planar surface having circuitry thereon surrounded by an unused reduced width buffer area;

a second planar surface opposite the first planar surface;

one or more perimeter sides extending between the first planar surface and the second planar surface; and

at least one perimeter side having two or more offset planar perimeter surfaces, each of the two or more offset planar perimeter surfaces being ground or polished surfaces without substantially any irregularities that produce weak points in the substrate, with one of the offset perimeter planar surfaces extending from the first planar surface and another of the offset perimeter planar surfaces extending from the second planar surface.

36. (Original) The semiconductor die as recited in claim 35, wherein each of the two or more offset planar perimeter surfaces is transverse to the first planar surface and the second planar surface .

37. (Original) The semiconductor die as recited in claim 35, wherein the semiconductor die has a substantially rectangular shape.

38. (Original) The semiconductor die as recited in claim 35, wherein the two or more offset planar perimeter surfaces are parallel.

39. (Original) The semiconductor die as recited in claim 35, wherein each of the two or more offset planar perimeter surfaces are polished surfaces.

41. (Currently Amended) A semiconductor die comprising:

a substrate having a first planar surface having an unused reduced width buffer area;

a second planar surface opposite the first planar surface;

one or more perimeter edges transverse to and extending between the first planar surface and the second planar surface; and

at least one perimeter edge having two or more offset planar surfaces, where the offset planar surfaces are substantially transverse to the first planar surface or the second planar surface with one of the offset planar surfaces extending from the first planar surface and the other of the offset planar surfaces extending from the second planar surface; and

each offset planar surface having a ground or polished surface without substantially any irregularities that produce weak points in the substrate.

42. (Original) The semiconductor die as recited in claim 41, wherein the semiconductor die comprises a rectangular die.

43. (Previously Presented) The semiconductor die as recited in claim 41, wherein each perimeter edge includes offset planar surfaces that are substantially parallel to one another, each of the offset planar surfaces on each perimeter edge are substantially transverse to the first planar surface and the second planar surface with one of the offset planar surfaces extending from the first planar surface and the other of the offset planar surfaces extending from the second planar surface.